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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,738	01/25/2002	Gilbert Wolrich	10559-618001/P12857	2797

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EXAMINER	
GU, SHAWN X	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/057,738	WOLRICH ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,13,16-21,26-29,33-35,37,40,41,43-45 and 49-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,26-29,33-35,37,40,41,43,45 and 57-60* is/are allowed.

6)☒ Claim(s) *13,16-21,44 and 49-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/22/06, 12/01/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 22 November 2006 and 1 December 2006 were filed after the mailing date of the Application on 25 January 2002. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Response to Amendment

2. This Office action is in response to the Request for Continued Examination filed 22 November 2006. Claims 1-7, 13, 16-21, 26-29, 33-35, 37, 40, 41, 43-45 and 49-60 are pending. Claims 1-7,26-29,33-35,37,40,41,43,45 and 57-60 have been allowed. All objections and rejections not repeated below are withdrawn.

Claim Objections

3. Claim 56 is objected to because of the following informalities:

"programming agent" should be changed to "processing agent".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13, 16-21, 44 and 49-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claims 13, 49 and 52, the words "permitting" renders the claims' metes and bounds unclear, since the claims would appear to cover anything and everything that does not prohibit the actions from occurring.

All dependent claims are rejected as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13, 16-19, 44, 49, 50, 52, 53, 55 and 56 are rejected under 35 U.S.C 103(a) as being unpatentable over Singhal et al. [5,978,874] (hereinafter "Singhal"), in further view of Misra et al. [US 6,654,836 B1] (hereinafter "Misra").

Per claims 13, 49, 52, 55 and 56, Singhal teaches a system comprising:

a plurality of memory resources [e.g., Data Out Buffer ("DOB") 186 and Data In Buffer ("DIB"), col. 29, lines 59-62; bcopy buffers or streaming IO buffers, col. 16, lines 50-55] each memory resource being associated with a memory controller [189, fig. 3];

a processing agent [180, fig. 2; Address Controller 180 generates control signals that are carried over path 190 to the Data Controller 140. Signal timings on the DataBus 70, the AddressBus/State Bus 60, the Arbitration Bus 80, and the Data ID Bus 90 are designed to permit such multiplex-partitioning of data and address paths, col. 6, lines 23-29] to access the memory resources;

a single bus to push data from the memory resources to the processing agent ;

a push bus arbiter [col. 16, lines 62-65] to arbitrate use of **the bus** by the memory resources, the memory resources obtaining access to **the bus** based on arbitration by the push bus arbitrator;

a single bus to receive data from the processing agent and to transfer the data to the memory resources;

and a pull bus arbiter to arbitrate use of-**the bus** by the memory resources. the memory resources obtaining access to **the bus** based on arbitration by the pull bus arbiter.

Singhal does not teach a system and a method for arbitrating data between the processing agent [e.g., Initiator] and the memory resource [e.g., Responder] using two different buses: a Push bus and a Pull bus; and unidirectionally transferring data from one of the memory resources to the processing agent through the push bus during a read phase, or unidirectionally transferring data from the processing agent to one of the memory resources through the pull bus during a write phase.

It would have been obvious for one having ordinary skill in the art at the time the invention was made to use two different buses for arbitrating data between the processing agent [e.g., Initiator] and the memory resource instead of a single bus in order to reduce number of turn-around cycles per bus, because the request and associated data are generally not sent on the same bus. Furthermore, the bandwidth in a two-bus connection is increased significantly over the single bus. The advantages of

multiple buses considerably increase memory bandwidth and increase data throughput via multiple data passages.

Furthermore, Misra teaches a controller having separate parts to handle read and write operations [see Fig 3] and a shared unidirectional pull bus (write data bus) and a shared unidirectional push bus (read data bus) [see Fig 2] in order to allow the controller to perform read and write operations at the same time [see column 3, lines 45-50]. Misra further teaches a read data phase and a write data phase in which the read and write operations are performed [see Fig 4], and such phases are the result of having a bus controller/arbiter in order to regulate the transfer of data between two devices. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Misra's teachings with those of Singhal for the above reasons. As a result of the combination, it is also made clear that the push bush only permits data to be sent from the memory resources and the pull bus only permits data to be sent from the processing agent as the buses are unidirectional. It is also clear that combining Misra's buses with Singhal's system would result in each board having separate read data bus and write data bus to the on board memory, while a shared read bus and a shared wite bus which are common to the boards are used for making requests to each other. An arbiter must be present when there is a possibility of multipe requests contending for access to a shared bus, and when there is a possibility of multiple requests arriving at a receiver simultaneously. Therefore, combined Misra and Singhal clearly indicates that separate read data bus arbiter and write data bus arbiter must be present on each board.

It is also clear that claims 55 and 56 are already described but claims 13, 49, 52.

Per claims 16 and 17, Singhal teaches the claimed limitations as mentioned above, and further teaches establishing a plurality of contexts on the programming agent [read/write-type transactions].

Singhal does not teach a plurality of program counters and a plurality of context relative registers, in which the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory DRAM input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers.

However, it would have been obvious for one having ordinary skill in the art at the time the invention was made to employ all circuitries as mentioned above into Singhal's computer system. These circuitries are well known in the art as hardware components which are used in instructions/transactions execution and storage.

Per claims 18 and 50, Singhal further teaches the programming agent executes a context and issues a read command to a memory controller to read data from one of the memory resources in a read phase [read-type transaction, col. 12, lines 47-65].

Per claim 19, Singhal further teaches the memory controller processes the read command to be sent to one of the memory resources [read-type transaction, col. 12, lines 47-60].

Per claim 44, Singhal further teaches the memory resources comprise memory controller channels [Fig. 3, 179, 185, 220,186, 187; col. 6, lines 51-65].

Per claim 53, Singhal further teaches the method of 52 further comprises operating the executing a context and issuing a write command to a memory controller to write data to one of the memory resources [write-back, col. 16, lines 3-12].

8. Claims 20, 21, 51 and 54 are rejected under 35 U.S.C 103(a) as being unpatentable over Singhal [5,978,874] and Misra [US 6,654,836 B1], in further view of Dennin et al. [US 6,401,149 B1] (hereinafter "Dennin").

Per claims 20, 51 and 54, Singhal in further view of Misra teaches the claimed limitations as noted above. Singhal does not teach the context is swapped out if the read data or if the write command is required to continue the execution of the context.

Dennin teaches a context switching process in which context or task is swapped out or in if a current read or write operation is idling for its arrival data [col. 9, lines 44-50; col. 10, lines 43-60]. It would have been obvious for one having ordinary skill in the art at the time the invention was made to swap out the lower priority context in order to

execute the higher priority context because the lower priority context is idle and inactive while waiting for requested data arrival. One would be motivated to process the active context while the other context is idle and inactive for the purpose of increasing system performance [col. 2, lines 45-60].

Per claim 21, Singhal inherently teaches after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer register of the programming agent, wherein after the data has been pushed, the programming agent reads the data in the input transfer register and the programming agent continues the execution of the context. This is because in the context switching process, the controller [the initiator] can process million instructions/transactions [read/write transaction] per second (MIPS) at a speed faster than a memory can provide data to the transactions. The output of the transactions after being processed must be stored in a transfer register such as buffer, read/write queue(s) and queued (delay read/write transaction) in the transfer register until the program agent [the responder] is ready to pull the output from the transfer register.

Allowable Subject Matter

9. Claims 1-7, 26-29, 33-35, 37, 40, 41, 43, 45 and 57-60 are allowed.

Response to Arguments

10. Applicant's arguments filed 22 November 2006 have been fully considered but they are not persuasive. The claims are taught by Singhal in further view of Misra and Dennin as set forth above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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12 January 2007